REMARKS

In identifying elected Claims 17 - 19 as being the only claims that are still pending in the application, the Examiner appears to have overlooked the remaining claims (Claims 1 - 16 and 20 - 24) which are still pending even though they have been not been examined.

Moreover, the Examiner has erred in withdrawing Claims 22 - 24 from consideration. Those claims depend from Claim 17, and since dependent claims include all of the elements of their parent claims, parent claims and dependent claims cannot be mutually exclusive, and without mutual exclusiveness, restriction is not proper.

As requested by the Examiner, Claims 17 and 18 are being rewritten with line indentations, and the Claim 18 is being further amended to refer to the stacked pair as "the vertically stacked pair".

Claims 17 - 19 have been rejected under 35 U.S.C. §112 as being indefinite because of the terms "near" in Claim 17 and "relatively thin" and "relatively thick" in Claim 19. Reconsideration is requested.

Contrary to the Examiner's suggestion, "near" is not a relative term that renders the claim indefinite. The term is widely used in patent claims, and if the Examiner has any authority supporting her position, she is requested to provide it. In Claim 17, the term is used in its normal sense as meaning close to, and in the specification and drawings, the select gates 44 and the bit line diffusions 50 are positioned on opposite sides of a dielectric film which has a thickness on the order of 120Å - 500Å. See Figs. 2 and 4C - 4E, and Page 6, lines 22 - 27. Hence one skilled in the art would be clearly apprised as to the scope of the claim.

In Claim 19, the terms "relatively thin" and "relatively thick" are used in relation to each other, and they simply mean that the "relatively thick" dielectrics are thicker than the "relatively thin" tunnel oxide. Here again, there is no ambiguity or indefiniteness.

Claims 17 - 19 have also been rejected under 35 U.S.C. §102 as being anticipated by Wong (U.S. 5,615,510). There is a major difference between applicant's invention and the device shown in Wong. In applicant's invention, the cell is a planar cell, whereas the device shown in Wong is a vertical cell.

Claim 17 distinguishes over Wong in calling for the steps of forming a vertically stacked pair of floating and control gates on a substrate, with the control gate being positioned above and aligned with the floating gate, forming a source diffusion in the

substrate on one side of the stacked pair, forming an erase gate above the source diffusion on the one side of the stacked pair, forming a select gate on a second side of the stacked pair, and forming a bit line diffusion in the substrate near the select gate. In that regard, it will be noted that the control gates are actually the portions of the polysilicon 1009 designated by the reference numeral 1021 in Figure 10E and that the portion labeled "control gate" is actually a word line that interconnects the control gates. Control gates 1021 extend axially within floating gates 1005. They are not stacked vertically with the floating gates, and they are not positioned above them. Similarly, source region 1002 is not formed in the substrate on one side of a stacked pair, and select gates 1022 are formed beneath control gates 1021, not to the side as claimed. Moreover, there are no bit line diffusions are formed in the substrate, and no bit line diffusions are formed near a select gate. Without these steps, Wong does not anticipate, and the rejection is clearly erroneous.

Claims 18 and 19 depend from Claim 17 and are directed to patentable subject matter for the same reasons as their parent claim. In addition, they further distinguish in calling for additional steps that are not found in Wong.

Claim 18 further distinguishes in calling for the steps of forming a bit line which crosses above the stacked pair, the erase gate and the select gate, and forming a bit line contact which interconnects the bit line diffusion and the bit line. In Wong, bit lines 1004 are formed on the substrate, they do not cross over a stacked pair, and there are no bit line diffusions and no contacts which interconnect bit line diffusions and bit lines. The Examiner is mistaken in suggesting that bit line contacts are inherent in the structure shown in Wong.

Claim 19 further distinguishes over Wong in calling for the steps of forming a relatively thin tunnel oxide between the floating gate and the substrate, a first relatively thick dielectric between the floating gate and the select and erase gates, and a second relatively thick dielectric between the floating gate and the control gate. In characterizing dielectric 1008 as a tunnel oxide between floating gate 1005 and substrate 1003, and dielectric 1008 and oxide layer 1019 as a first relatively thick dielectric between floating gate 1005 and select gate and erase gates 1022, 1018, the Examiner has tried to use dielectric 1008 both as a relatively thin tunnel oxide and as a relatively thick dielectric, which she cannot do. She is further mistaken in characterizing oxide layer 1019 as a first relatively thick dielectric between floating gate 1005 and select gate and erase gates

1022, 1018. Oxide layer 1019 is not between floating gate 1005 and either an erase gate or a select gate, but rather between bit line 1004 and erase/program gate 1018.

In view of the substantial differences between the invention defined by the claims that have been examined and the reference, applicant trusts that the rejection will be withdrawn and that Claims 17 - 19 will be allowed. As the Examiner has noted, Claim 17 is generic, and with the allowance of the generic claim, the other claims (Claims 1 - 16 and 20 - 24 should be allowed as well and the application should be in condition for allowance.

The Commissioner is authorized to charge any fees required in this matter, including extension fees, to Deposit Account 50-2975, Order No. A-75031-1.

Respectfully submitted,

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